REMARKS

Claims 1, 4, 6, 8, 11 and 17 have been amended, claim 28 has been added and claims 3 and 15 have been canceled. Claims 1, 2, 4 and 6 to 28 are now active in this application. Please charge any costs to Deposit Account No. 20-0668.

Claims 1 to 27 were rejected under 35 U.S.C.103(a) as being unpatentable over Arimoto et al. (U.S. 6,232,793) in view of Kaplinsky (U.S. 5,568,062). The rejection is respectfully traversed.

Claim 1 requires, among other features, a logic circuit which includes a pair of complementary serially connected MOS transistors coupled between a voltage supply source and a reference voltage source, the transistor coupled to the reference voltage source having a lower leakage and driving current than the other of the complementary serially connected MOS transistors. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references either alone or in the combination as claimed. This feature minimizes leakage current during standby as stated in the specification.

Claim 1 further requires a bias voltage supply circuit which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the other of said complementary serially connected MOS transistors. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references either alone or in the combination as claimed. This feature minimizes leakage current during standby as stated in the specification.

Claims 2, 4, 6 and 7 depend from claim 1 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 1.

In addition, claim 2 further limits claim 1 by requiring that the bias voltage supply circuit include a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and the first or second bias voltage being output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 4 further limits claim 3 by requiring that said other of the MOS transistors of the logic circuit be a PMOS transistor and the other transistor of said logic circuit be an NMOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 6 further limits claim 1 by requiring that one bias voltage be above the threshold voltage of said other of the complementary serially connected MOS transistors and the other bias voltage be below the threshold voltage of said other of the complementary serially connected MOS transistors. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 7 further limits claim 1 by requiring at least one additional logic circuit coupled to the bias voltage supply circuit. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 8 requires, among other features, a logic circuit having a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of the second MOS transistor being permanently coupled to ground potential, the second transistor having a lower leakage and driving current than the other of the complementary serially connected MOS transistors. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 8 further requires a bias voltage supply circuit which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claims 9 to 16 depend from claim 8 and therefore define patentably over the applied references for at least the reasons discussed above with reference to claim 8.

Claim 9 further limits claim 8 by requiring that the first MOS transistor be a PMOS transistor and the second MOS transistor be an NMOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 10 further limits claim 8 by requiring that the first bias voltage be lower than the second bias voltage. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 11 requires, among other features, a logic circuit having a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of the second MOS transistor being permanently coupled to ground potential, the second transistor having a higher threshold voltage than the first MOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 11 further requires a bias voltage supply circuit which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 12 further limits claim 8 by requiring that the first bias voltage be lower than the second bias voltage. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 13 further limits claim 8 by requiring that the bias voltage supply circuit include a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and the first or second bias voltage be output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 14 further limits claim 13 by requiring that the MOS transistor of the logic circuit be connected to the first voltage supply line. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 15 further limits claim 14 by requiring that the MOS transistor of the logic circuit and the first MOS transistor and second MOS transistor be PMOS transistors. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 16 further limits claim 15 by requiring that the logic circuit include an NMOS transistor connected between the PMOS transistor and a third voltage supply line. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 17 requires, among other features, a logic circuit having a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, the second transistor having a lower leakage and driving current than the other of the complementary serially connected MOS transistors. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references either alone or in the combination as claimed.

Claim 17 further requires a first bias voltage supply circuit which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 17 still further requires a second bias voltage supply circuit which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the second MOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claims 18 to 27 depend from claim 17 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 17.

In addition, claim 18 further limits claim 17 by requiring that the first MOS transistor be a PMOS transistor and the second MOS transistor be an NMOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 19 further limits claim 17 by requiring that the first bias voltage from the first bias supply circuit be lower than the second bias voltage from the first bias supply circuit. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 20 further limits claim 17 by requiring that the first bias voltage from the second bias supply circuit be lower than the second bias voltage from the second bias supply circuit. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 21 further limits claim 17 by requiring that the first MOS transistor have a lower threshold voltage than the second MOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 22 further limits claim 17 by requiring that the first bias voltage supply circuit include a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line and the first or second bias voltage be output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 23 further limits claim 17 by requiring that the second bias voltage supply circuit include a third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a fourth MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a first bias supply line. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 24 further limits claim 17 by requiring that the first bias voltage supply circuit include a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line and the first or second bias voltage be output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor and that the second bias voltage supply circuit include a third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a fourth MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a third bias supply line. No such

feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 25 further limits claim 22 by requiring that the first and second MOS transistors of the first bias voltage supply circuit be PMOS transistors. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 26 further limits claim 23 by requiring that the first and second MOS transistors of the second bias voltage supply circuit be NMOS transistors. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 27 further limits claim 22 by requiring that the first and second MOS transistors of the first bias voltage supply circuit be PMOS transistors and the first and second MOS transistors of the second bias voltage supply circuit be NMOS transistors. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

Claim 28 further limits claim 11 by requiring that one of the bias voltages be above the threshold voltage of the first MOS transistor and the other of the bias voltages be below the threshold voltage of the first MOS transistor. No such feature is taught or suggested by Arimoto et al., Kaplinsky et al. or any proper combination of these references in the combination as claimed.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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Jackie McBride

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